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PATENT

NPO-20535-2-CU
Application No. 10/768,754

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Stoica, et al.

Serial No. 10/768,754

Group Art Unit: 2128

Filed: January 26, 2004

For: EVOLUTIONARY TECHNIQUE FOR AUTOMATED SYNTHESIS OF ELECTRONIC CIRCUITS

Examiner: Fred O. Ferris III

DECLARATION UNDER RULE 1.131

I, Adrian Stoica, do hereby declare and say as follows:

I am a Principal Research Engineer at the Jet Propulsion Laboratory (JPL), where I have worked since February 1996. I have MS and PhD degrees in Electronics and Computer Engineering and have over 20 years of research experience in adaptive and learning hardware including reconfigurable and evolvable hardware. I organized and was Chair of the first US meeting in evolvable hardware, the NASA/DOD Conference on Evolvable Hardware, which started in 1999 and has become the main event in the field. I am author of over 100 papers.

Being a named inventor on the present invention, I am extremely familiar with the development dates of said invention.

As can be seen by the dates on the attached invention disclosure, a description of the present invention prepared on September 4, 1998 and information regarding development of the invention was submitted to my employer, the California Institute of Technology at the Jet Propulsion Laboratory and received by them on September 8, 1998. As described in the invention disclosure, the invention had been completely reduced to practice prior to these dates..

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All statements made herein are of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, I understand that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

A. Stoica

Adrian Stoica

Date: 10/10/2006

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CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION LABORATORY
TECHNOLOGY REPORTING AND COMMUNICATIONS (TRAC)
Novel Technology Report

NASA CASE NO.	20535
JPL ITEM NO.	01326

FROM: Adrian Stoica Section: 344 Ext.: 4-2190 Employee #: 07278

The following is a possible invention or item of novel technology:
TITLE: Evolutionary technique for automated synthesis of electronic circuits

OWNERSHIP FACTORS: (Check applicable items)
This item is related to or resulted from:

☒ Assigned work; or the expectation, in doing my job, that I will:

☐ Originate new JPL projects, tasks, proposals, RTOPS, etc. ...; or

☒ Recognize and propose solution(s) to technical problems whether or not assigned; or

☐ Other (Explain) _____

FUNDING DISCLOSURE:

FUNDING SOURCE (CHECK): ☒ NASA ☐ DOD ☒ DOE ☐ Tech. Affiliates ☐ SBIR, STTR ☐ BMDO ☐ TCA

☐ OTHER (Specify): _____

☐ Corporate Sponsor: _____ Contact: _____

TASK ORDER NO./AMENDMENT NO.: _____

JPL INVENTOR(S)

If more than one inventor has been named, the Innovation must have resulted from interaction between the Innovators, and each must have made a creative contribution. State of the art design, mathematical analysis (unless implemented in software), experimentation, tool making, etc., are not innovative or inventive.

PERSONAL INFORMATION	SPECIFIC INVENTIVE CONTRIBUTION
(1) Name Adrian Stoica Ext. 4-2190 Employee # 07278 Citizenship Australia Supervisor Anil Thakoor Address 64 Harkness Ave. #1, Pasadena, CA 91106	Had the original idea of using the proposed circuit architecture and the evolutionary search algorithm.
(2) Name Carlos Harold Salazar-Lazaro Ext. 4-9513 Employee # 08599 Citizenship Venezuela Supervisor Anil Thakoor Address 1749 Siskiou Blvd. #7, Ashland, OR 97520	Contributed to the refinement of the search algorithm and its implementation in software
(3) Name _____ Ext. _____ Employee # _____ Citizenship _____ Supervisor _____ Address	
(4) Name _____ Ext. _____ Employee # _____ Citizenship _____ Supervisor _____ Address	

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NON-JPL INVENTOR(S)

PERSONAL INFORMATION (First Initial Last)	COMPANY / UNIVERSITY	PHONE	CITIZEN-SHIP	RESIDENTIAL ADDRESS
(1) Name _____ Contribution _____				
(2) Name _____ Contribution _____				
(3) Name _____ Contribution _____				

If any inventors are non-JPL employees, specify/describe how the collaboration occurred, e.g., subcontractor (give contract no., TCA), former student, former employee, collaboration at a scientific conference, etc.:

HISTORICAL DATA	DATE	LOCATION
a. Conception	04/19/97	300-308
b. Disclosure to Others	04/02/98	303-313
c. First Sketch or Drawing	03/10/97	300-308
d. First Written Description	03/10/97	300-308
e. Completion of Model or Fully Developed Device	03/20/98	300-308
f. First Test or Operation	03/20/98	300-308

Results of Test Evolved circuits with a desired response characteristic (a bell-shaped output at a ramp input)

Related Reference Reports Regarding State of the Art Technology

1. Thompson, A. Silicon Evolution. In: Proceedings of Genetic Programming 1996 (GP96), J.R. Koza et al. (Eds), pages 444-452, MIT Press 1996

2. Koza, J., Bennett III, F. H., Lohn J., Dunlap, F., Keane M. A., and Andre, D. "Automated Synthesis of Computational Circuits Using Genetic Programming". In Proc. of Second Annual Genetic Programming Conference, Stanford July 13-16, 1997

COMMERCIALIZATION FACTORS

A. Is this invention ready for commercialization in its current form? If not explain. Is the commercializable form different from the invention's current form? In what way(s)? Yes.

B. At what level of development is the invention? What further development is necessary or ongoing? Prototype developed? Invention fixed in its final form?
The invention has been demonstrated on a sequence of software prototypes (including prototypes that are very accurate models of hardware). A chip implementing the proposed architecture is currently under fabrication. The invention is in final form.

C. Specify applications/markets and estimated use in commercial market place (be very specific, e.g., automobile, semiconductor, etc.). What is the intended/ anticipated use of the invention?
The main market would be design automation, the semiconductor industry, consumer electronics, aerospace. The relevance in design automation and semiconductor industry relates to the capability of automatically evolving new circuit designs, from target specifications. In aerospace or consumer electronics applications, the use would be in achieving adaptive hardware, i.e. electronics that self-adapt to changing environments.

D. What companies are developing and marketing products in this technology area (i.e., possible competitors to your invention)? What are these products?
Companies like Xilinx and Altera develop various field-programmable logic devices, which could be used to support searches directly in hardware.

E. List any related/similar government applications which currently utilize similar technology or over which your invention is an improvement.
None.

F. List any companies or government agencies with potential interest in this innovation. List the names and phone numbers of any people you have contacted or who have contacted you concerning this invention.
BMDO, DARPA , DOD in general, Texas Instruments, Analog Devices

G. What other methods are there for performing the function of the invention? Differentiate your invention over the other methods and, if possible, discuss your advantages/disadvantages. Attach any additional pages if necessary.
There are no other existing methods that perform the same function as the described invention. The proposed invention relates with techniques described in References [1] and [2]. The main difference compared to [1] is that our invention specifies an architecture which can evolve analog electronic circuits, while the work described in [1] is restricted to digital circuits. The main difference compared to [2] is that our invention is a solution to making chips that can implement the solution determined by evolution (and in fact evolution can be done directly on the chip, with orderes of magnitude increased speed and and with guarrantied performance, which does not depend on accurate simulators), while the work described in [2] is not directly implementable in hardware.

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SEMICONDUCTOR MICROELECTRONIC DEVICE

Is the technology a semiconductor chip product? If so, is it in the form of a mask work and is the mask work fixed in its final form?
No.

PATENT RIGHTS STATUS

A. Has a written description of this invention been submitted or accepted for printed publication? Do you plan on submitting it for publication in the future? Or, have copies been distributed to others external to JPL? If so, please identify by title, date, journal or other publication vehicle or place.
No submission for publication has yet been made. We plan to submitt it to IEEE Transaction on Evolutionary Computation sometime in October.

B. Have any disclosures been made without a nondisclosure agreement? Do you plan on a future public disclosure? To Whom? When? If disclosures have been made with a nondisclosure agreement in place, provide a copy of the nondisclosure agreement or other applicable agreement, such as a TCA or TAP agreement.
No disclosures have been made outside our Group. We plan to disclose it at two Conferences in September. One is Military and Aerospace applications of Programmable Devices and Technologies (MAPLD) Conference at NASA Goddard, Sept 15-16, and the other is Int. Conf. on Evolutionary Computation in Lausanne, Switzerland, Sept 23-26

C. Has any form of the technology involved been sold or offered for sale? If so, please give dates and conditions under which the sale or offer has been accomplished.
No.

D. Has the technology involved been built or used for its intended commercial purpose? If so, please give dates and particulars.
No.

NASA TECH BRIEFS

Do you consider NASA Tech Briefs a proper forum for the dissemination of this disclosure? If so, why? (If published in Tech Briefs, a technical support package, consisting solely of this NTR, will be provided upon request to interested U.S. industry representatives. Therefore, please be as complete as possible, providing any applicable photos, figures, text, or supporting documentation.) Please note, the tech brief will not be published until a patent determination has been made and the inventor has approved the text of the Tech Brief.
Yes. It is a novel technology that would interest a large audience of users of electronics, and could have an impact on how electronics are designed and can achieve real world adaptation..

NTR INVENTOR'S REPORT

NASA CASE NO. 132 20535
JPL ITEM NO.

PLEASE BE AS CLEAR AND SPECIFIC AS POSSIBLE, AS THIS REPORT MAY BE MADE AVAILABLE THROUGH TECH BRIEFS

Sections 1 (Novelty), 2A (Problem), and 2B (Solution) must be completed fully. Your published paper may be attached to satisfy Section 2C (Description and Explanation).

1. Novelty - Describe what is new and different about your work and its improvements over the prior art.
Evolution of analog circuits means automated circuit synthesis, through a sequence of gradually better solutions. Our invention allows evolution of hardware implementable analog electronic circuits and, moreover, evolution directly in hardware, on-the-chip. Related work (described in [2]) in evolving electronic circuits relies on ideal components, and has not addressed hardware implementation issues; the methods used in previous work do not extend to allow a hardware implementation of the underlying architecture for evolving directly in hardware. Another related work ([1]) addressed evolution directly in hardware, but was limited to evolution on existing programmable digital devices; currently there are no analog chips capable of evolution.

2. Technical Disclosure

   A. Problem - Motivation that led to development or problem that was solved.
   Evolution in hardware (directly on the chip), can speed-up the search for a solution circuit by a few orders of magnitude compared to evolution in software simulations. Moreover, since the software simulation relies on models of physical hardware with certain limited accuracy, a solution evolved in software may behave differently when downloaded in programmable hardware; such mismatches are avoided when evolution takes place directly in hardware. This invention offers a solution for evolution directly in hardware.

   B. Solution
   The solution to achieving evolution in hardware was the choice of FET transistors (NMOS and PMOS) as the basic elements for circuit design, and the design of a reconfigurable architecture in which the interconnections between the transistors are programmable (the architecture has similarities with FPGA architectures, in which interconnections between logical cells are programmable).The second aspect of the solution is the use of an evolutionary/genetic algorithm to search in the space of possible circuit configurations.

   C. Detailed Description and Explanation
   See the attached paper. The architecture consists of a certain arrangement of MOS transistors and a set of interconnections between some of their terminals. The interconnections are controlled by the search algorithm.The solution if the search algorithm determines a circuit topology that produces the desired response.

September 4, 1998

Evolutionary Design of Electronic Circuits

By Adrian Stoica and Carlos Salazar-Lazaro

Evolutionary Design/Synthesis of Electronics

Evolutionary techniques (Genetic Algorithms, Genetic Programming) have been proposed for automated synthesis of electronic hardware. The idea is to employ a search/optimization algorithm that operates in the space of possible circuits and determines a circuit/solution with a desired response. For example, one may try to synthesize a filter with a certain frequency response characteristic or a computational circuit with a certain DC characteristic. The main steps of evolutionary synthesis are illustrated in Figure 1.

---Insert Figure 1 here---

First, a population of individuals ("chromosomes" corresponding to circuits) is generated randomly. The chromosomes are then converted into circuit models (if the evolution takes place in simulations, a.k.a. "extrinsic" evolution) or control bitstrings downloaded to programmable hardware (if the circuits are evaluated directly in hardware, a.k.a. "intrinsic" evolution). In extrinsic evolution a simulator evaluates the models, while in intrinsic evolution the hardware itself produces a physical response to the input signal(s). The response/behavior of the circuits is compared with a desired/target response, and the individuals are ranked according to how close their response comes to the desired response. Closing the cycle, a new population of individuals is generated from a selected pool of best individuals in the previous generation, subject to a set of genetic operators such as chromosome crossover and mutation. The process is repeated for many generations, and results in increasingly better individuals. The stopping criteria may be reducing the error below a certain threshold, or reaching a predetermined number of generations. One or several solutions may be found among the individuals of the last generation.

Several people have brought important contributions to the domain of evolutionary design of electronics but only two works are mentioned to illustrate essential ideas related to this report.

- Koza and colleagues at Stanford U. used Genetic Programming to grow an "embrionic" circuit to a circuit that satisfies desired requirements. This approach was used for evolving filters, computational circuits, etc. Koza's evolutions were performed in simulations, *without the concern of a physical implementation*, but rather as a proof-of-concept that evolution can lead to designs which compete or even exceed in performance the human designs. No analog programmable devices exist that would support the implementation of the resulting design (but, in principle, one can test their validity in circuits built from discrete components, or in an ASIC), and thus intrinsic evolution was not possible.
- Thompson at Sussex U. in U.K. achieved intrinsic evolution on a programmable digital device – a Field Programmable Gate Array (FPGA). He used a Genetic Algorithm to evolve a frequency discriminator from the digital gates available on a small part of the FPGA.

We propose an approach related with the above techniques, in which an evolutionary algorithm searches in the space of circuits configurable on a Programmable Transistor Array (PTA). The PTA allows synthesis of analog, digital and mixed-signal circuits. The PTA allows thus extending Thompson's work on digital circuits to analog designs. Compared to Koza's work our approach offers a mean for implementing the solution determined by evolution in a programmable chip. Moreover, evolution can be done directly on the chip, with orders of magnitude increased speed and with guarantied performance (unlike the case when a solution is found in simulations but certain silicon/fabrication effects impede observing the same response in the hardware implementation).

Programmable Transistor Array (PTA)

The proposed PTA is an array of transistors interconnected by programmable switches. The status of the switches (On or Off) determines a circuit topology and consequently a specific response. Thus, the topology can be considered as a function of switch states, and can be represented by a binary sequence such as "1011..." where by

convention one can assign 1 to a switch turned On and 0 to a switch turned Off. The PTA can be a modular architecture, in which a certain module can be cascaded/expanded to determine a more complicated circuit topology. Figure 2 illustrates an example of a PTA module consisting of 8 transistors and 24 programmable switches. In this example the transistors P1-P4 are PMOS and N5-N8 are NMOS, and the switch based-connections are in sufficient number to allow a majority of meaningful topologies for the given transistors arrangement, yet less than the total number of possible connections.
---Insert Figure 2 here---

Programming the switches On and Off determines a circuit for which in a first approximation the effects of non-zero, finite impedance of the switches can be neglected. An example of a circuit drawn with this simplification is given in Figure 3. The thicker lines are non-programmable connections to power supply, input signals and output measuring instrument. The thin lines are short-circuit connections (the corresponding switches are Off/open) between transistor terminals, while the dotted lines signify open connections (the corresponding switches are On/closed).
---Insert Figure 3 here---

In a realistic model the switches have a non-zero resistance/impedance in the On state, and a big, but finite, resistance in the Off state. While the effects of non-perfect switches may be negligible for most common applications of digital circuits, such effects may fundamentally affect analog programmable circuits. As an example, the circuits shown in Figure 4 are outside normal design practices e.g. the transistors P1 and P2 have floating gates (in theory infinite resistance between the gates). In reality, when a switch between the two gates is Off, the resistance is not infinite but finite (~ Mohm or Gohm), and the responses of the circuits in Figure 4 are very similar (under certain test conditions) to that of the circuit shown in Figure 3 (the On resistance is also not zero, but rather ~ tens of Ohms).
---Insert Figure 4 (a,b) here---

Evolution on the PTA
This section details the evolution of a circuit with a gaussian I-V DC response. The algorithm illustrated in Fig. 1 was applied to the model of PTA illustrated in Fig. 2. The evolution was simulated on a Caltech supercomputer (HP-Exemplar), with the parallel PGAPACK [ ] code for the Genetic Algorithm, and the public domain version of SPICE 3F5 as a circuit simulator. Successful evolution was demonstrated on multiple runs with populations between 50 and 512 and 50 to 100 generations. The execution time depends on the above variables and on the number of processors used (commonly 64 out of the 256 available), but was on average of the order of 20 minutes (the same evolutions took about 2 days on a SUN SPARC 10). The solutions found include the circuits illustrated in Figure 4, which produce the first two responses in Figure 5; some other responses from the same generation are illustrated for comparison.
---Insert Figure 5 here---

Conclusion
This paper presents a method of evolutionary synthesis of electronic circuits. A Programmable Transistor Array is proposed as the reconfigurable structure on which an evolutionary algorithm can search for circuit solutions satisfying desired characteristics. The method was demonstrated in simulations and a chip was sent for fabrication.

References:
1. Thompson, A. Silicon Evolution. In: Proceedings of Genetic Programming 1996 (GP96), J.R. Koza et al. (Eds), pages 444-452, MIT Press 1996
2. Koza, J., Bennett III, F. H., Lohn J., Dunlap, F., Keane M. A., and Andre, D. "Automated Synthesis of Computational Circuits Using Genetic Programming". In Proc. of Second Annual Genetic Programming Conference, Stanford July 13-16, 1997

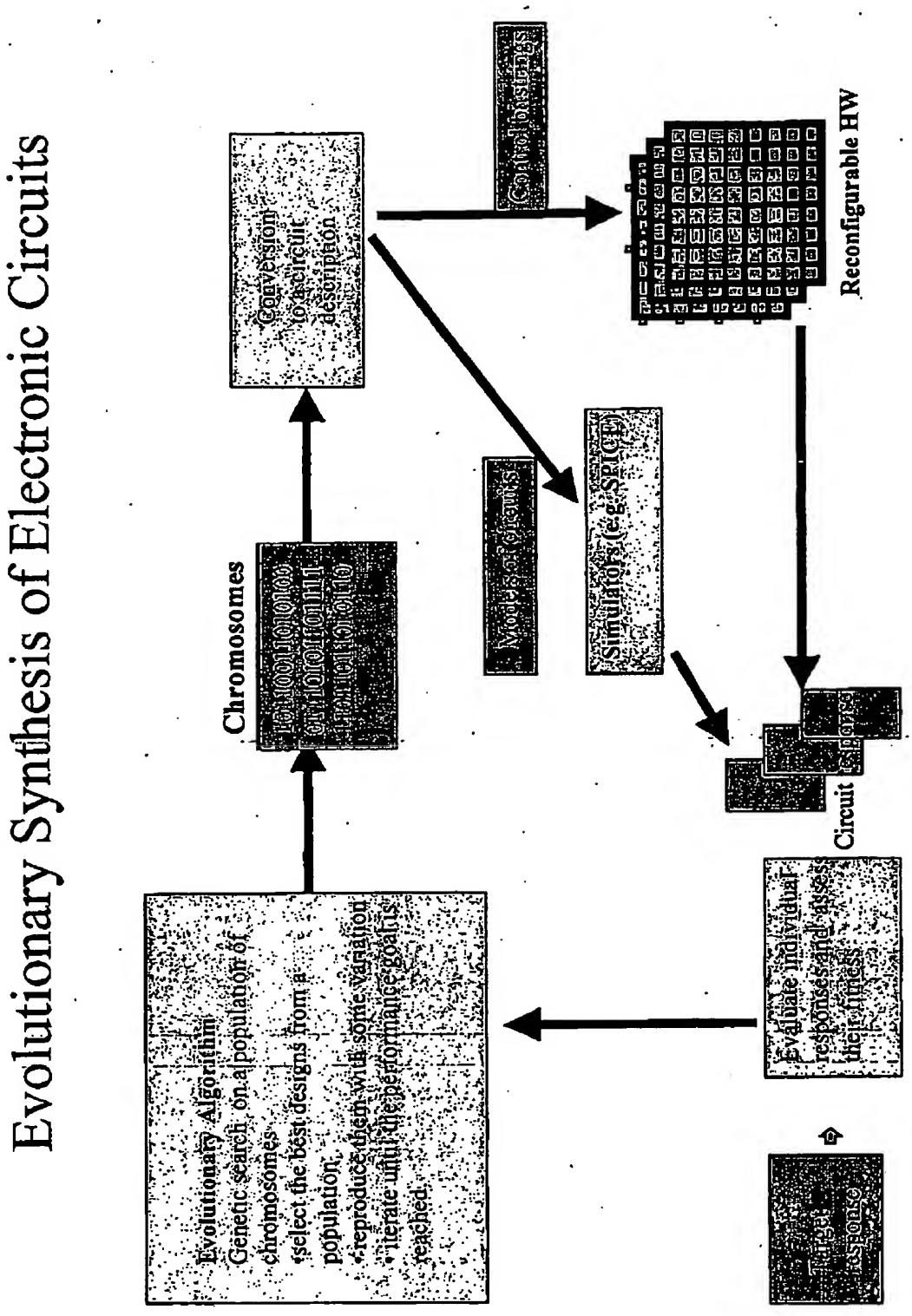

Fig 1.

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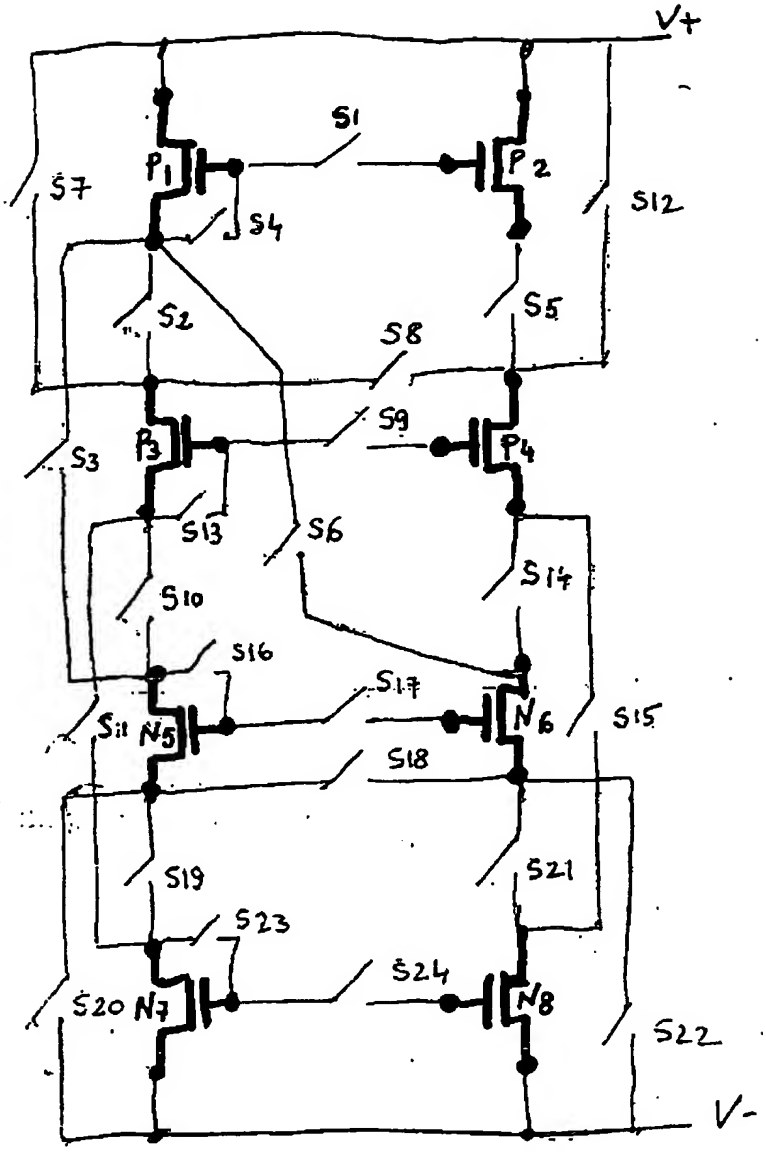
V+
S1
P1
P2
S7
S4
S12
S2
S5
S8
S9
P3
P4
S3
S13
S6
S14
S10
S16
S17
N6
S15
S11
N5
S18
S19
S21
S23
S24
S20
N7
N8
S22
V-

Fig 2

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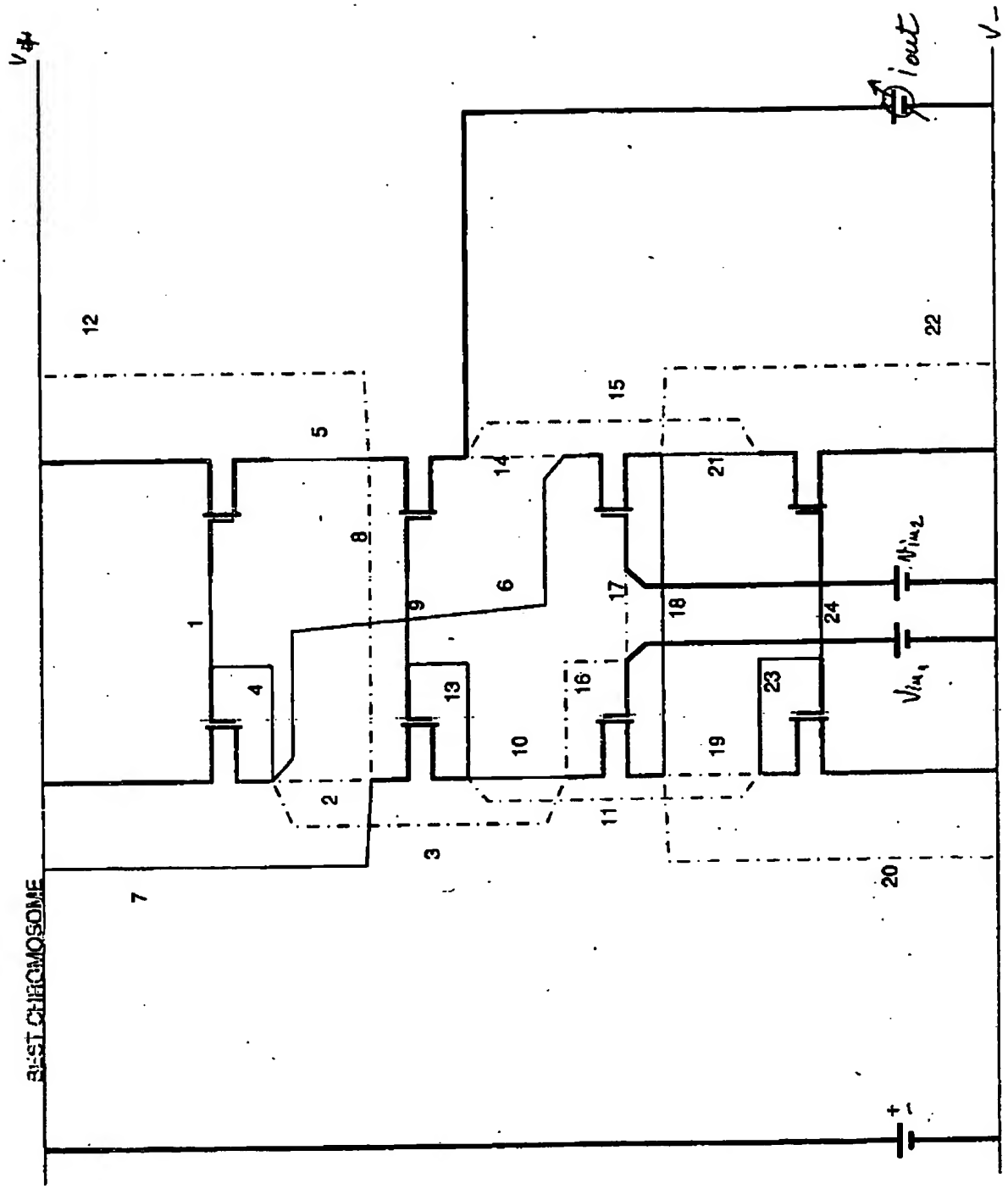

Fig 3

Without_annealing_pop_ctrl.ps

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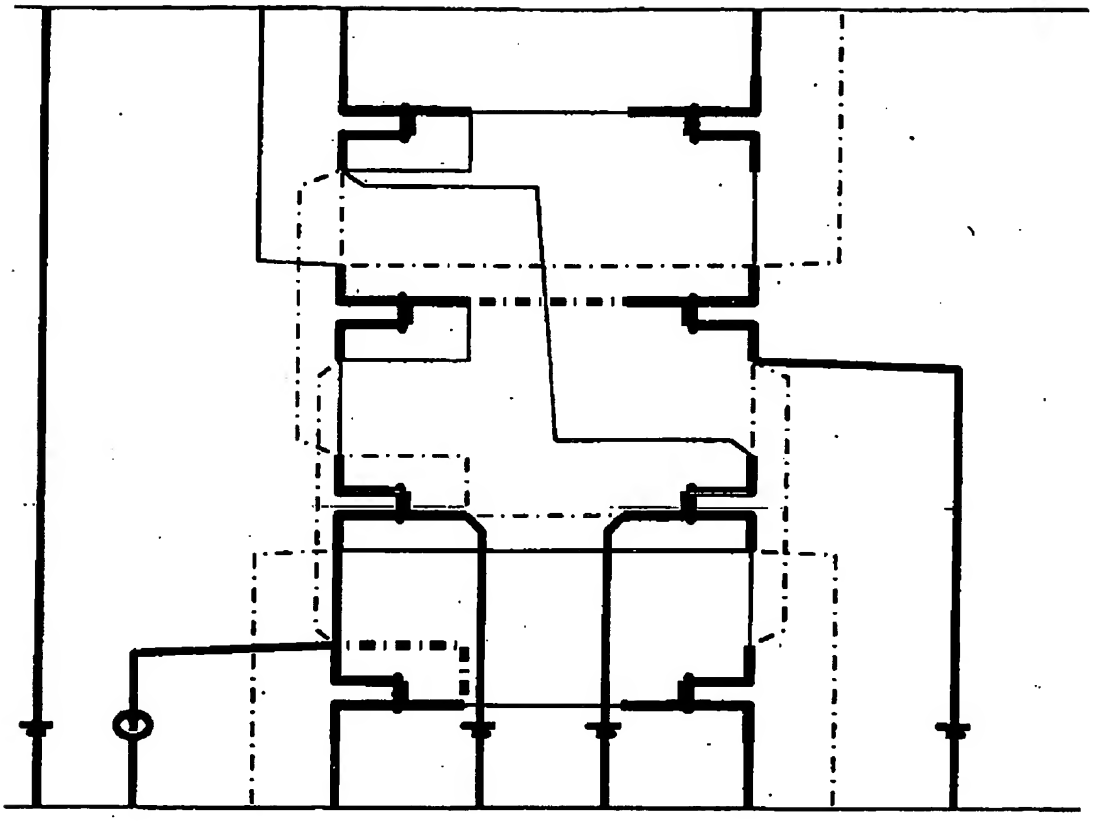

Fig 4_9

without-annealing-pop-civ2.ps

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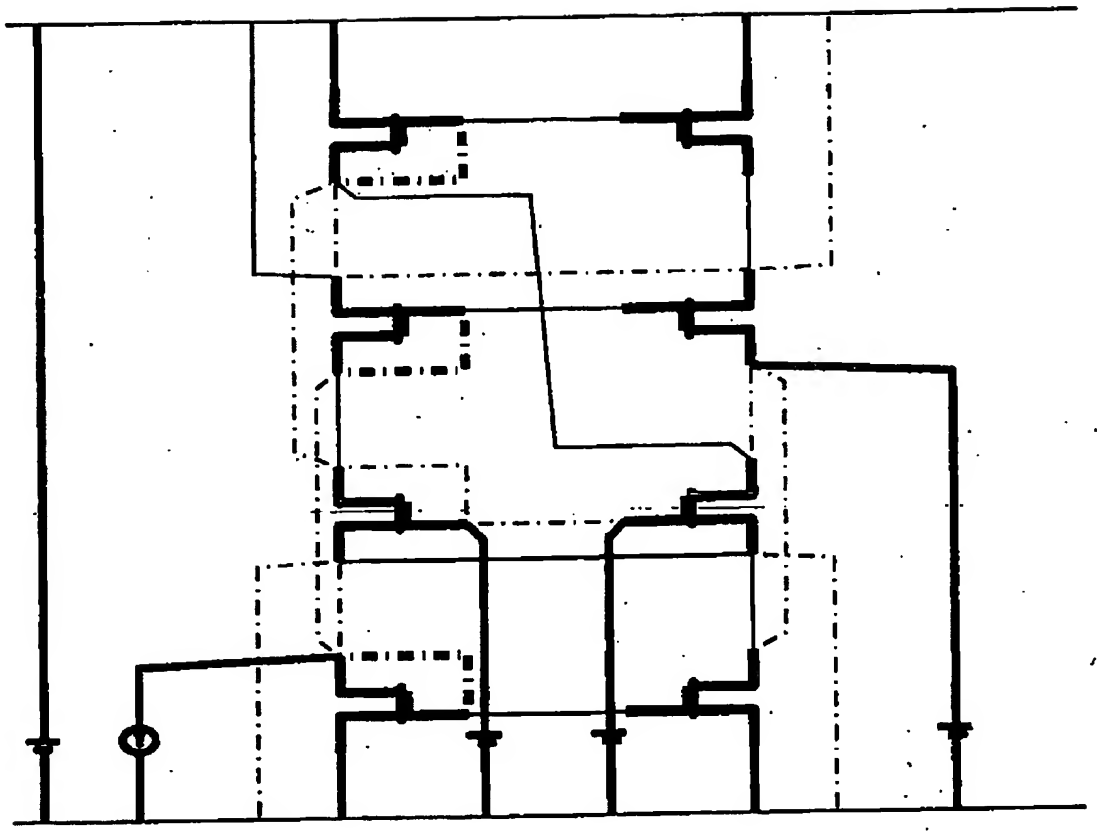

Fig 4.6

Without_annealing_pop.ps

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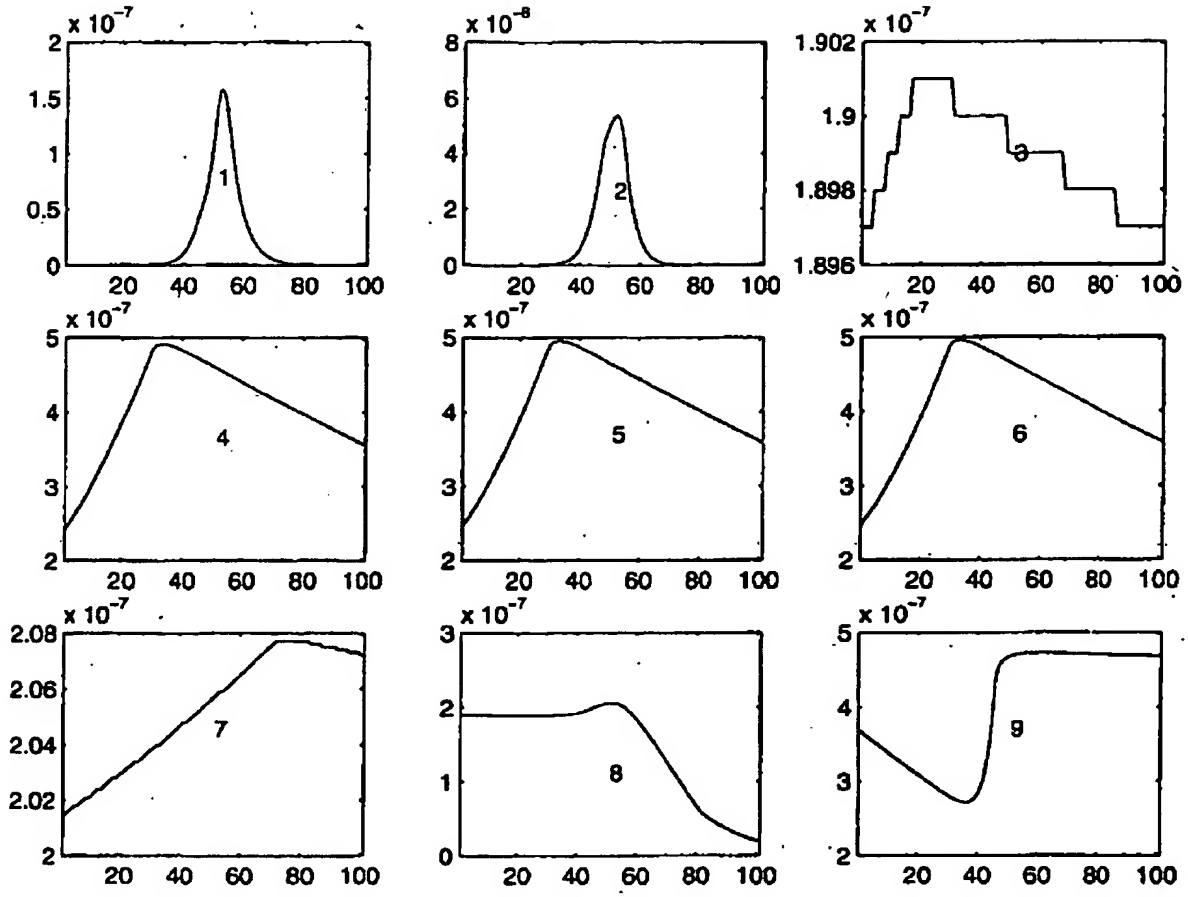

Fig 5.